UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,218	07/14/2006	Erik J. Marinissen	NL04 0065 US1	2749

65913 7590 06/04/2008

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2117	

NOTIFICATION DATE	DELIVERY MODE
06/04/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/586,218	MARINISSEN ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☒ Claim(s) *1-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a non-Final Office Action in response to the present US Application 10/586218, filed 07/14/2006, which is a national stage entry of PCT/IB05/50153 international Filing Date: 01/13/2005.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file, for the EUROPEAN PATENT OFFICE (EPO) Application No. 04100141.3, filed 01/19/2004.

The drawings received on 7/14/2006 are not acceptable, for the reasons as set forth in the present Office Action.

The replacement Abstract submitted on 6/26/2007, in response to the Notice of Non-Compliant Amendment dated June 5, 2007, is acceptable.

Claims 1-25 are presently under examination and pending.

Drawings

Figures 1, 2A, 2B, 3A and 3B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "A test access architecture and method for modular testing a system on chip (SOC)". Appropriate correction is required.

Claim Objections

Claims 1-25 are objected to because of the following informalities with respect to claims language. Some of the language in the limitations should be changed accordingly to better define the claimed invention.

Claim 1, -- A test access architecture for testing modules in an electronic circuit, the test access architecture comprising:

a test access mechanism arranged to transport test stimulus data and test response data to and from a module under test, respectively;

a global enable signal provided for placing the modules in a test mode; and

a control circuit provided between the global enable signal and an associated module, wherein the control circuit is arranged to control passing of the global enable signal to the associated module.--

The claims are generally narrative and indefinite, failing to conform to current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. Similar language

informalities associated with claim 1 may exist in other claims. Specifically, Applicant should pay attention to claimed expressions, "such that" in claims 13 and 23, and "pipelined manner" in claims 10 and 23, respectively. These expressions are indefinite and should be deleted or amended appropriately to more clearly define the invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Corbin et al. (US Patent No. 7,103,814) filed: October 25, 2002.

Regarding independent Claims 1, 13, Corbin discloses an apparatus and method for testing logic and embedded memory in a semiconductor integrated circuit device using test access architecture (logic scan chain) located on the same chip, comprising:

a test access mechanism (scan chains) arranged to load logic test patterns and unload test results via the scan chains while the BIST engine is running during testing of the semiconductor integrated circuit device, Figs. 2 and 3.

A global enable signal (scan test enable) for placing the semiconductor integrated circuit in the scan test.

a control circuit (general purpose test register latch 40) receives the scan test enable signal and provides a control signal ("bypass") to a multiplexer 50 (scan chain bypass isolation element) in each memory segment. The control signal "bypass" from the test latch 40 puts the MUX 30 into bypass mode by selecting the scan in signal, not the output 44 of the BIST engine. Logic patterns can then be loaded and results unloaded via the scan chains while the BIST engine is running. When the BIST is done, the bypass MUX 50 is taken out of the bypass mode and the results can be unloaded via the scan chains using a clocking scheme.

Regarding Claims 2-4, 14-16, Corbin discloses control circuit (general purpose test register latch 40) receives the scan test enable signal and provides a control signal ("bypass") to a multiplexer 50 (scan chain bypass isolation element) in each memory segment. The control signal "bypass" from the test latch 40 puts the MUX 30 into bypass mode by selecting the scan in signal, not the output 44 of the BIST engine.

As shown in Fig. 3, once the BIST patterns are loaded, the chip is put into bypass mode 53 (memory macros are isolated from the scan chains) via the bypass signal shown in FIG. 2. In bypass mode, independent BIST test clocks are generated by the process described in section 2. Logic test patterns are loaded and results unloaded via scan chains in parallel with the BIST engine running 54.

Regarding Claims 5-9, 17-22, Corbin discloses general purpose test register latch 40, which is used to provide a control signal (labeled "bypass") to a multiplexer 50

in each memory segment. The test register latch 40 is located within the (scan chains) associated with each memory macro portion 23 of the chip under test 20, located on the same chip under test, Figs. 1 and 2.

Regarding Claim 10-12, 23-25, Corbin discloses scan chains, using independent clocking for the logic and the memory test sequences, arranged to load the logic test patterns and unload the test results, while the BIST engine is running during testing of the semiconductor integrated circuit device, Figs. 2 and 3. During scan operations, the clocks enable the global test clocks so that BIST contents can be properly unloaded (scanned out).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMES C KERVEROS/
Primary Examiner, Art Unit 2117

Date: 3 June 2008
Office Action: Non-Final Rejection

U.S. Patent & Trademark Office
Alexandria, VA 22314.
Tel: (571) 272-3824, Fax: (571) 273-3824
Email: james.kerveros@uspto.gov